

INTERVIEW SUMMARY

Applicant's representative held a telephonic conference with Examiner Pizarro-Crespo on December 17, 2002. Applicant's representative would like to express his great appreciation for Examiner Pizarro-Crespo providing the time to discuss issues regarding the Office Action mailed September 24, 2002 (paper no. 26) (hereinafter Office Action).

Independent claims 1 and 63 were discussed. Moreover, proposed amendments to independent claims 1 and 63 were presented to Examiner Pizarro-Crespo and discussed. While no agreement was reached, the Examiner stated that the amendments to the claims may move the case forward to allowance, but he could not give a definitive statement of allowance without a more thorough review of the amendment language in the context of the art of record.

Independent claims 1 and 63 are amended in the following response with the exact amendment language presented and discussed with Examiner Pizarro-Crespo on December 17, 2002.

REMARKS

Claims 1 and 63 are amended with the exact amendment language presented and discussed with Examiner Pizarro-Crespo on December 17, 2002. Favorable examination of these claims is respectfully requested.

Claims 15-16 are canceled, new claims 73-80 are added. Claims 1, 4-14 and 56-80 are pending in the application.

Claims 69 and 70 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which is not disclosed in the specification. Claim 10 stands rejected under 35 U.S.C. §112, fourth paragraph, as being an improper dependent claim. Claims 63, 71 and 72 stand rejected under 35 U.S.C. §102 as being anticipated by Deboer (U.S. Patent No. 5,930,106). Claims 1, 4-11, 13-15, and 56 stand rejected under 35 U.S.C. §103 as being unpatentable over Ramakrishnan (U.S. Patent No. 5,192,871). Claims 12 and 16 stand rejected under 35 U.S.C. §103 as being unpatentable over Ramakrishnan and further in view of Graettinger (U.S. Patent No. 5,844,771). Claims 57-59 stand rejected under 35 U.S.C. §103 as being unpatentable over Ramakrishnan in view of Narui (U.S. Patent No. 6,201,728) and Merchant (U.S. Patent No. 6,235,594). Claims 60-62 stand rejected under 35 U.S.C. §103 as being unpatentable over Ramakrishnan in view of Eguchi (U.S. Patent No. 5,442,585) and Shrivastava (U.S. Patent No. 5,557,122). Claims 64-68 stand rejected under 35 U.S.C. §103 as being unpatentable over Deboer in view of

Anderson (U.S. Patent No. 5,390,072).

Regarding the §112, first paragraph, rejection against claims 69-70, the Examiner states that the limitation "the high-K dielectric layer has at least a portion comprising less than or equal to 98% crystalline material" is not supported by the original disclosure because it contains no lower limit percentage. Claims 69-70 are amended to include a lower limit of the range, and therefore, this rejection is rendered moot. Applicant respectfully requests withdrawal of such rejection against claims 69-70 in the next Office Action.

Regarding the rejection against claim 10 based on §112, fourth paragraph, the Examiner states that the phrase "the high K substantially crystalline material layer is at least 98% crystalline" is inconsistent with claim 1 from which claim 10 depends. Claim 10 is amended to delete such language, and therefore, the rejection is rendered moot. Applicant respectfully requests withdrawal of this rejection in the next Office Action.

Regarding the obviousness rejection against claim 1 based on Ramakrishnan, such claim recites wherein the high K substantially crystalline material layer is at least 70% crystalline and less than 90% crystalline. The Examiner alleges that Ramakrishnan teaches a crystalline dielectric layer of 100% crystalline (page 12 of paper no. 26). In no fair or reasonable interpretation does such alleged teaching of Ramakrishnan teach or suggest a high K substantially crystalline material layer that is at least 70% crystalline and **less**

than 90% crystalline. Accordingly, Ramakrishnan, singularly or in any combination, fails to teach a positively recited limitation of claim 1, and therefore, claim 1 is allowable. Applicant respectfully requests allowance of claim 1 in the next Office Action.

Claims 4-14, 56-62 and 80 depend from independent claim 1, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Regarding the obviousness rejection against claims 57-59 based on the combination of Ramakrishnan '871 in view of Narui and Merchant, the claims recite an insulative layer intermediate a substrate and first and second capacitor electrodes. The Examiner states Narui teaches an insulative layer between the substrate and a capacitor to minimize current leakage, with Merchant teaching the insulative layer is silicon dioxide (pg. 8 of paper no. 26). Accordingly, the Examiner is suggesting modifying the Ramakrishnan invention by the teachings of Narui to form an insulative layer between the substrate and capacitor disclosed in Ramakrishnan. However, this modification would destroy the function of the Ramakrishnan invention, contrary to Federal Circuit and MPEP authority.

The Examiner is respectfully reminded that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended

purpose, then there is no suggestion or motivation to make the proposed modification. MPEP §2143.01 (8th Edition) *citing to In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Ramakrishnan teaches a first electrode of capacitor 10 is an epitaxial layer 14 **that is grown from the surface of substrate** 12. Accordingly, if one modified the Ramakrishnan invention as suggested by the Examiner to provide an insulative layer between the capacitor, or first electrode, and substrate, the epitaxial could not be grown, and therefore, the capacitor could not be formed destroying the Ramakrishnan invention. Pursuant to the above authority, since the proposed modification would render the Ramakrishnan invention unsatisfactory for its intended purpose, there is no suggestion or motivation to make the proposed modification, and therefore, the obviousness rejection is improper and fails. For at least reason, the obviousness rejection must be withdrawn and claims 57-59 allowed.

Moreover, the Examiner is respectfully reminded that if the proposed modification or combination of the prior art would change the principal of operation in the prior art invention being modified, then the teachings of the reference are not sufficient to render the claims *prima facie* obvious. MPEP §2143.01 (8th Edition) *citing to In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The court in *In re Ratti* reversed a rejection holding the “suggested combination of references would require substantial reconstruction and redesign of elements shown in the [primary reference] as well as a change in the basic

principle under which the [primary reference] construction was designed to operate" 270 F.2d at 813, 123 USPQ at 352. To modify the Ramakrishnan invention as suggested by the Examiner would require substantial reconstruction and redesign of elements shown in the Ramakrishnan invention as well as a change in the basic principle under which the Ramakrishnan invention construction was designed to operate because the capacitor would have to be redesigned **not to include** an epitaxial layer as a first electrode layer. Such a redesign is improper pursuant to the above authority, and therefore, for this additional reason, the obviousness rejection is improper and fails. For this additional reason, the obviousness rejection must be withdrawn and claims 57-59 allowed.

Regarding the anticipation rejection against claim 63 based on Deboer, such claim recites a first electrode layer formed within an opening and having *a portion most proximate and spaced from an upper surface of a substrate*, the portion elevationally below the uppermost surfaces of two gate structures. Deboer teaches a first or bottom electrode 21 which contacts an upper surface of substrate 10 (Figs. 2-4). In no fair or reasonable interpretation does Deboer, singularly or in any combination, teach a first electrode formed within an opening and having a portion most proximate and **spaced from** an upper surface of a substrate, the portion elevationally below the uppermost surfaces of two gate structures. Accordingly, Deboer, singularly or in any combination, fails to teach

a positively recited limitation of claim 63, and therefore, claim 63 is allowable.

Applicant respectfully requests allowance of claim 63 in the next Office Action.

Claims 64-79 depend from independent claim 63, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

For example, new claim 73 recites a conductive region intermediate the first electrode layer and substrate, the conductive region electrically connecting the first electrode layer and substrate. Deboer teaches a first electrode layer that directly contacts a substrate, without any intermediate conductive region. Accordingly, Deboer, singularly or in any combination, fails to teach a positively recited limitation of claim 73, and therefore, claim 73 is allowable.

New claims 74-78 recite to materials for the conductive region recited in claim 73. Since Deboer fails to teach any such conductive region, it is inconceivable that such reference, singularly or in any combination, could teach the recited limitations of claims 74-78. New claims 74-78 are allowable.

Claim 79 recites a first electrode layer comprising conductively doped polysilicon. Deboer teaches a storage or bottom electrode can be formed as conductively doped germanium-silicon or as a metal base electrode (col. 3, lines 20-34). In no fair or reasonable interpretation does Deboer, singularly or in any combination, teach a first electrode layer comprising conductively doped

polysilicon as recited in claim 79. Claim 79 is allowable. Applicant respectfully requests allowance of claim 79 in the next Office Action.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed together with this application on September 21, 2000. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "A Version with markings to show changes made."

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 12-24-02

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Att. to
Paper No. 27

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/512,149
Filing Date February 23, 2000
Inventor Vishnu K. Agarwal
Assignee Micron Technology, Inc.
Group Art Unit 2814
Examiner Marcos Pizarro-Crespo
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry Including A Capacitor With An Amorphous And A Crystalline
High K Capacitor Dielectric Region

VERSION WITH MARKINGS TO SHOW CHANGES MADE
ACCOMPANYING RESPONSE TO SEPTEMBER 24, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions
and ~~strikeouts~~ indicate deletions.

1. (Amended) Integrated circuitry comprising a capacitor comprising a
first capacitor electrode, a second capacitor electrode and a high K capacitor
dielectric region received therebetween; the high K capacitor dielectric region
comprising a high K substantially amorphous material layer and a high K
substantially crystalline material layer, the high K substantially amorphous material
and the high K substantially crystalline material constituting different chemical
compositions, the high K substantially crystalline material being received over the
high K substantially amorphous material; and

wherein the high K substantially crystalline material layer is at least 70%
crystalline and less than 98% 90% crystalline.

10. (Amended) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous, ~~and the high K substantially crystalline material layer is at least 98% crystalline.~~

63. (Amended) Integrated circuitry comprising:

a substrate having ~~insulative material formed over an upper surface the substrate; and~~

at least two gate structures laterally spaced from one another and formed over the upper surface of the substrate, the two gate structures having uppermost surfaces;

insulative material formed over the two gate structures and the upper surface of the substrate;

an opening formed in the insulative material between the two gate structures; and

a capacitor comprising:

a first electrode layer formed within the opening and having a portion most proximate and spaced from the upper surface of the substrate, the portion elevationally below the uppermost surfaces of the two gate structures;

a high K dielectric layer formed over the first electrode layer and within the opening; and

a second electrode layer formed over the high K dielectric layer.

69. (Amended) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising greater than 70% and less than or equal to 98% crystalline material.

70. (Amended) The integrated circuitry of claim 63 wherein the high K dielectric layer has at least a portion comprising greater than 70% and less than or equal to 98% amorphous material.

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